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for

METHOD OF GENERATING AN EFFICIENT STUCK-AT FAULT AND TRANSITION DELAY FAULT TRUNCATED SCAN TEST PATTERN FOR AN INTEGRATED CIRCUIT DESIGN

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METHOD OF GENERATING AN EFFICIENT STUCK-AT FAULT AND TRANSITION DELAY FAULT TRUNCATED SCAN TEST PATTERN FOR AN INTEGRATED CIRCUIT DESIGN

5   BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is directed to testing
and screening of integrated circuit dies to detect
10   defective devices. More specifically, but without
limitation thereto, the present invention is directed to
a method of screening defective dies to achieve maximum
stuck-at fault and transition delay fault test coverage
for an integrated circuit design.

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2. Description of Related Art

Scan based methods for stuck-at fault (SAF)and
transition delay fault (TDF) testing of integrated
circuit dies generally requires a large number of test
20   patterns to achieve satisfactory test coverage, in some
cases, more than 30,000 patterns. Previous methods to
reduce the pattern count include inserting logic into the
integrated circuit design to perform data compaction,
however, this method requires extra resources and added
25   cost. Another method is launch-off shift TDF pattern
generation, in which the test pattern transitions are
launched during shift. The launch-off shift method has
been proven to reduce the number of TDF patterns with
higher fault coverage, however, the launch-off shift

method requires routing the global scan enable as a clock having a well-controlled insertion delay relationship with all other clocks in the integrated circuit design, which may not be practical in some integrated circuit

5   designs.

SUMMARY OF THE INVENTION

In one aspect of the present invention, a

10   method of generating a truncated scan test pattern for an integrated circuit design includes steps of:

(a) receiving as input an integrated circuit design;

(b) estimating a number of transition delay fault test patterns and a corresponding number of top-off

15   stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage;

(c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set

20   of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and

(d) generating as output the truncated set of

25   transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns.

In another aspect of the present invention, a computer program product for generating a truncated scan test pattern for an integrated circuit design includes:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

5   (a) receiving as input an integrated circuit design;

(b) estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage;

10   (c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum

15   stuck-at fault and transition delay fault coverage within a selected scan memory limit; and

(d) generating as output the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures,

25   in which like references indicate similar elements throughout the several views of the drawings, and in which:

FIGS. 1A, 1B, 1C and 1D illustrate a flow chart of a method of truncating transition delay fault test

patterns according to an embodiment of the present invention;

FIG. 2 illustrates a table of values used to generate the plot of FIG. 3;

5   FIG. 3 illustrates a plot of stuck-at fault coverage as a function of the stuck-at fault test pattern number according to an embodiment of the present invention;

FIGS. 4A and 4B illustrate a table of values
10   used to generate the plot of FIG. 5; and

FIG. 5 illustrates a plot of stuck-at fault coverage as a function of the test pattern number for the transition delay fault test patterns according to an embodiment of the present invention.

15   Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some elements in the figures may be exaggerated relative to other elements to point out distinctive features in the
20   illustrated embodiments of the present invention.

DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Frequency dependent defects in integrated
25   circuit die that result in severe timing failures are typically referred to as transition delay faults (TDF). Historically, transition delay faults have been screened using at-speed or high-speed functional testing of the die. Due to the cycle time required during the design

phase, however, it is desirable to generate a screening
method for transition delay faults using scan chains.
The number of possible test patterns that may be used for
both stuck-at fault (SAF) and transition delay fault (TDF)

5   test patterns is determined by the size of the scan
memory available in standard production testing
equipment.

Transition delay fault test patterns also
detect stuck-at faults. Accordingly, transition delay

10   fault patterns are preferably generated first to detect
both stuck-at faults and transition delay faults. The
transition delay fault patterns may then be analyzed to
determine the stuck-at fault coverage, and the remaining,
or top-off, stuck-at fault patterns may be generated to

15   achieve maximum fault coverage for both stuck-at faults
and transition delay faults. Unfortunately, however, the
total number of fault patterns generated may exceed the
scan memory limit of the testing equipment.

In a method of the present invention, the

20   number of transition delay fault test patterns is
truncated to leave enough scan memory for the top-off
stuck-at fault pattern, while still achieving maximum
fault coverage.

In one aspect of the present invention, a

25   method of generating a truncated scan test pattern for an
integrated circuit design includes steps of:

(a) receiving as input an integrated circuit design;

(b) estimating a number of transition delay fault
test patterns and a corresponding number of top-off

stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage;

(c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and

(d) generating as output the truncated set of transition delay fault patterns and the corresponding number of top-off stuck-at fault patterns.

The steps of estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns and truncating the estimated number of transition delay fault test patterns are further detailed in the flow chart of FIG. 1.

FIGS. 1A, 1B, 1C and 1D illustrate a flow chart 100 of a method of truncating transition delay fault test patterns according to an embodiment of the present invention.

Step 102 is the entry point of the flow chart 100.

In step 104, an integrated circuit design is received as input, and the maximum number of scan test patterns for the integrated circuit design that may be accommodated by the current scan test equipment is calculated from the available scan memory. A portion of the available scan memory is preferably reserved for scan

quiescent current (IDDQ) and memory built-in self repair (BISR) scan tests.

A scan pattern requires both scan memory and functional (parallel) memory in the integrated circuit
5   design to store each scan pattern. The same amount of scan memory is required for either a stuck-at fault scan pattern or a transition delay fault scan pattern, however, an additional functional (parallel) memory location is required to store each transition delay fault
10   scan pattern. Fortunately, the size of the functional (parallel) memory is generally not a severe limitation in scan testing.

In step 106, a full set of stuck-at scan test patterns is generated according to well known techniques,
15   for example, by commercially available scan test pattern generation software. A full set of stuck-at scan test patterns is a set that can detect the maximum number of faults that may be detected in the integrated circuit design. Preferably, the scan test patterns are checked
20   and debugged, if necessary, to ensure that they pass best/worst case conditions for parallel and serial simulations. The number of faults that may be detected by each of the stuck-at fault scan test patterns is stored for each corresponding scan test pattern.
25   In step 108, the set of stuck-at fault scan test patterns generated in step 106 is re-ordered according to the number of stuck-at faults that each test pattern can detect. For example, if pattern "A" can detect 20 faults, pattern "B" can detect 8 faults,

pattern "C" can detect 25 faults, and pattern "D" can detect 12 faults, then the test patterns are re-ordered as "C" (25), "A" (20), "D" (12), "B" (8). The re-ordering of the stuck-at fault test patterns is an important feature

5   of the present invention.

In step 110, the stuck-at fault coverage is plotted as a function of the test pattern number in the re-ordered set of stuck-at fault test patterns.

FIG. 2 illustrates a table of values 200 used

10   to generate the plot of FIG. 3.

FIG. 3 illustrates a plot of stuck-at fault coverage 300 as a function of the stuck-at fault test pattern number according to an embodiment of the present invention. In the example of FIG. 3, approximately 90

15   percent fault coverage is achieved from the first 800 scan test patterns, while 3411 additional, or "top-off", test patterns are needed to the achieve the maximum fault coverage of 97.45 percent. The advantageously high fault coverage achieved from a relatively low number of test

20   patterns is a direct result of the re-ordering the test patterns described above.

In step 112, a list of faults that may be captured for each scan clock domain in the integrated circuit design is generated. Scan set and reset signals

25   that are declared as scan clocks are preferably constrained to their inactive values, since they do not capture transition faults into scan cells. Another list of faults is generated that contains faults that may not be captured by any of the scan clocks.

In step 114, a set of transition delay fault
scan patterns is generated for each scan clock domain by,
for example, commercially available scan test generation
software. The generated scan test patterns should be
5   able to run at functional speed for the launch and
capture cycles of a fault simulation run.

In step 116, if fewer than a selected number of
test patterns, for example, 200, are generated for a
corresponding scan clock domain, no truncation is
10   performed. If more than the selected number of test
patterns is generated for the corresponding scan clock
domain, then the total number of faults that may be
detected by each of the test patterns generated for the
corresponding scan clock domain is calculated. The set
15   of transition delay fault test patterns for each
corresponding scan clock domain is re-ordered according
to the number of faults that may be detected by each test
pattern as described above. The re-ordering of the
transition delay fault test patterns according to the
20   number of faults that each test pattern can detect is an
important feature of the present invention. Each set of
transition delay fault test patterns is truncated to
remove the test patterns that can detect, for example,
less than 10 percent of the total number of faults
25   calculated for the corresponding scan clock domain. The
test patterns in each set of transition delay fault test
patterns that can detect, for example, at least 90
percent of the total number of faults calculated for each
corresponding scan clock domain are retained. In the

fault simulation, all scan clocks are preferably enabled, however only the scan clock for the corresponding clock domain is enabled during launching and capturing the scan test patterns, and only the faults associated with the

5   scan clock for the corresponding clock domain are loaded. As a result, each fault simulation detects transition delay faults within the corresponding clock domain. For example, a fault that is launched by scan clock "A" is captured by scan clock "A". A list of the detected and

10   undetected faults in each fault simulation is saved for each corresponding scan clock domain.

         Empirical results show that using the truncated transition delay fault scan patterns that can detect at least 90 percent of the faults in each scan clock domain

15   screens out 99.9 percent of transition delay fault defect parts, while the total number of transition delay fault scan patterns is reduced by about 75 percent. While further truncation of the transition delay fault scan patterns may be required to fit into the scan memory of

20   the test equipment, the previous truncation of the transition delay fault scan patterns according to fault coverage ensures that the number of defective parts that may not be detected is kept to a minimum.

         In step 118, transition delay fault scan

25   patterns are generated for the remaining undetected faults and cross-clock domain faults.

         In step 120, if fewer than a selected number, for example, 200, test patterns are generated, no truncation is performed. If more than the selected

number of test patterns is generated, then the total number of faults that may be detected by all test patterns in the set is calculated. The set of transition delay fault test patterns for the remaining undetected

5   faults and cross-clock domain faults is re-ordered according to the number of faults that may be detected by each test pattern as described above. The set of transition delay fault test patterns is truncated to remove the test patterns that can detect, for example,

10   less than 10 percent of the calculated total number of faults that may be detected by the full set of test patterns. The test patterns in the set of transition delay fault test patterns that can detect, for example, at least 90 percent of the total number of faults that

15   may be detected by the full set of test patterns are retained.

In the fault simulation, all scan clocks are enabled during shifting, launching and capturing the scan test patterns. The list of faults that may not be

20   captured by any of the scan clocks that was generated in step 110 and the fault list saved in step 112 are loaded to detect transition delay faults across clock domains. For example, a fault that is launched by scan clock "A" may be captured by scan clock "B". The generated

25   transition delay fault test patterns should be simulated at the slowest scan clock speed for the launch and capture cycles.

In step 122, the total number of transition delay fault test patterns generated in steps 114 and 118 is calculated and saved for future reference.

5   In step 124, the sets of transition delay fault test patterns generated in steps 114 and 118 are evaluated to determine the stuck-at fault coverage using, for example, commercially available test software and test equipment.

10   In step 126, the sets of transition delay fault test patterns generated in steps 114 and 118 are ordered according to stuck-at fault coverage from the highest fault coverage to the least fault coverage to generate an ordered set. The ordering of the test pattern sets according to fault coverage results in improved stuck-at

15   fault coverage and is an important feature of the present invention.

In step 128, a plot of stuck-at fault coverage is generated as a function of the number of transition delay fault test patterns of the ordered set generated in

20   step 126.

FIGS. 4A and 4B illustrate a table of values 400 used to generate the plot of FIG. 5. The highlighted values of 2370 and 3714 represent the total number of transition delay fault patterns selected for all

25   individual clock domain test runs and the total number of transition delay fault patterns selected for all individual clock domain test runs plus all clock domain test runs, respectively.

FIG. 5 illustrates a plot of stuck-at fault coverage 500 as a function of the test pattern number for the transition delay fault test patterns according to an embodiment of the present invention. The importance of arranging the transition delay fault test patterns in order of fault coverage may be appreciated from the slope of the resulting curve in FIG. 5. The steps in the curve occur at the beginning of each different set of transition delay fault test patterns.

In step 130, the number of top-off stuck-at fault test patterns is estimated from an analysis of the plots generated from the tables in FIG. 2 and FIGS. 4A and 4B. In this example, it is assumed that the scan memory can accommodate a total of 7,000 test patterns.

A first estimate may be made as follows. From FIG. 4B, if the transition delay fault test patterns are truncated to 3650 test patterns, then the corresponding stuck-at coverage is 91.29 percent, and there is scan memory available for 3350 top-off test patterns. From FIG. 2, the closest lower test coverage to the estimated number of test patterns is 91.03 percent, and 3315 top-off stuck-at fault test patterns are required to achieve a maximum 97.45 percent test coverage for a total of 4211 test patterns. However, there is still scan memory available for (3350 - 3315 = 35) more test patterns before reaching the 7,000 test pattern limit. If insufficient scan memory is available, then a lower number of transition delay fault test patterns is selected.

A second estimate may be made as follows.
Because more scan memory is available, the number of
transition delay fault test patterns may be truncated to
3682 in FIG. 4B. The corresponding stuck-at coverage is

5   91.33 percent, and there is scan memory available for
3318 top-off test patterns. From FIG. 2, from 91.30
percent, 3283 top-off stuck-at fault test patterns are
required to achieve a maximum 97.45 percent test coverage
for a total of 4211 test patterns. However, there is

10   still scan memory available for (3318 - 3283 = 35) more
test patterns before reaching the 7,000 test pattern
limit.

A third estimate may be made as follows. From
FIG. 4B, if the transition delay fault test patterns are

15   truncated to 3714 test patterns, then the corresponding
stuck-at coverage is 91.35 percent, and there is scan
memory available for 3286 top-off test patterns. From
FIG. 2, from 91.30 percent, 3283 top-off stuck-at fault
test patterns are required to achieve a maximum 97.45

20   percent test coverage for a total of 4211 test patterns.
However, there is still scan memory available for (3286 -
3283 = 3) more test patterns before reaching the 7,000
test pattern limit.

A fourth estimate may be made as follows. From

25   FIG. 4, if the transition delay fault test patterns are
truncated to 3746 test patterns, then the corresponding
stuck-at coverage is 91.38 percent, and there is scan
memory available for 3254 top-off test patterns. From
FIG. 2, the closest lower test coverage to the estimated

number of test patterns is 91.03 percent, and 3283 top-off stuck-at fault test patterns are required to achieve 97.45 percent test coverage for a total of 4211 test patterns. However, the available scan memory is (3254 -

5   3283 = -29), therefore the scan memory lacks sufficient space for 29 top-off stuck-at fault test patterns.

A fifth estimate may be made as follows. From FIG. 4B, if the transition delay fault test patterns are truncated to 3778 test patterns, then the corresponding

10   stuck-at coverage is 91.42 percent, and there is scan memory available for 3222 top-off test patterns. From FIG. 2, from 91.30 percent, 3283 top-off stuck-at fault test patterns are required to achieve 97.45 percent test coverage for a total of 4211 test patterns. However, the

15   available scan memory is (3222 - 3283 = -61), therefore the scan memory lacks sufficient space for 61 top-off stuck-at fault test patterns.

The above analysis determines that the values for third estimate utilizes most of the scan memory and

20   is therefore the optimum estimate.

In step 132, if the total number of transition delay fault test patterns calculated in step 122 plus the number of top-off stuck-at fault test patterns estimated in step 128 is less than or equal to the maximum number

25   of allowed test patterns calculated in step 104, then all the transition delay fault test patterns and the stuck-at fault test patterns should fit into the scan memory of the current scan test equipment, and step 132 is followed

by step 140. Otherwise, step 132 is followed by step 134.

In step 134, the optimum number of transition delay fault test patterns is further truncated to make available sufficient scan memory to generate the top-off stuck-at fault test pattern to achieve the highest possible stuck-at fault coverage using the analysis described in step 128.

In step 136, the last set of transition delay fault test patterns is truncated so that only the selected test patterns remain to select as many transition delay fault test patterns as possible while still reserving sufficient scan memory for top-off stuck-at faults to achieve maximum stuck-at fault test coverage. For example, if there are 11 sets of transition delay fault test patterns, and 1344 out of 5920 test patterns are selected in the last set of test patterns, then only the first 1344 test patterns of the last test pattern set are saved. In some cases, there may be enough scan memory available so that fewer test patterns have to be removed from the last test pattern set.

In step 138, the truncated transition delay fault test patterns are fault graded for stuck-at fault coverage according to well known techniques. Both detected and undetected faults are saved.

In step 140, the top-off stuck-at fault test patterns are generated to achieve maximum fault coverage, loading only the undetected faults saved in step 136.

In step 142, if the total of the number of top-off stuck-at fault test patterns generated in step 140 plus the number of selected test patterns (either all the transition delay fault patterns or the truncated number

5   of transition delay fault patterns generated in step 136) does not exceed the maximum number of test patterns allowed, then all the transition delay fault test patterns and stuck-at fault patterns can fit into the scan memory, and step 142 is followed by step 144.

10   Otherwise, the transition delay fault test patterns must be further truncated by looping back to step 134.

In step 144, the selected transition delay fault test patterns and the top-off stuck-at fault patterns generated for stuck-at fault coverage are fault

15   graded for stuck-at coverage according to well known techniques. The result is the final stuck-at fault coverage for the integrated circuit design.

In step 146, the transition delay fault test patterns selected for transition delay fault coverage are

20   fault graded for transition delay fault coverage. The result is the final transition delay fault coverage for the integrated circuit design.

In step 148, a parallel fault simulation is performed for best and worst case conditions for all the

25   selected transition delay fault and stuck-at fault test patterns. If a pattern mismatch occurs, the corresponding test pattern is debugged.

In step 150, a serial fault simulation is performed for best and worst case conditions for some,

preferably at least five, of the transition delay fault and stuck-at fault test patterns. If a pattern mismatch occurs, the corresponding test pattern is debugged.

In step 152, other tests and checks may be performed for all the selected transition delay fault and stuck-at fault test patterns, for example, tester rules, bidirectional conflicts checking, and test program generation. If violations are detected, the test patterns may be debugged according to well known techniques.

In step 154, the final truncated transition delay fault scan test patterns and the corresponding number of top-off stuck-at fault scan test patterns that can fit into the scan memory is generated as output.

Step 156 is the exit point of the flow chart 100.

In another aspect of the present invention, a computer program product for generating a truncated scan test pattern for an integrated circuit design includes:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input an integrated circuit design;

(b) estimating a number of transition delay fault test patterns and a corresponding number of top-off stuck-at fault patterns to achieve maximum stuck-at fault and transition delay fault coverage;

(c) truncating the estimated number of transition delay fault patterns to generate a truncated set of transition delay fault patterns so that the truncated set of transition delay fault patterns and the corresponding

5   number of top-off stuck-at fault patterns achieve maximum stuck-at fault and transition delay fault coverage within a selected scan memory limit; and

(d) generating as output the truncated set of transition delay fault patterns and the corresponding

10   number of top-off stuck-at fault patterns.

Although the method of the present invention illustrated by the flowchart descriptions above are described and shown with reference to specific steps performed in a specific order, these steps may be

15   combined, sub-divided, or reordered without departing from the scope of the claims. Unless specifically indicated herein, the order and grouping of steps is not a limitation of the present invention.

While the invention herein disclosed has been

20   described by means of specific embodiments and applications thereof, numerous modifications and variations could be made thereto by those skilled in the art without departing from the scope of the invention set forth in the following claims.

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